APPARATUS, METHOD AND SYSTEM FOR ACCELERATED GRAPHICS PORT BUS BRIDGES

Abstract of the Disclosure

A computer system having at least one central processing unit, system memory, and a core logic capable of accepting an AGP bus is provided with an AGP to AGP bridge connected to the standard AGP bus. The AGP to AGP bridge can accommodate two or more AGP-compatible devices that can be accessed through the standard AGP bus via the AGP to AGP bridge. A PCI to memory bridge is also provided within the AGP to AGP bridge so that PCI devices may be connected to the AGP to AGP bridge. The AGP to AGP bridge is fitted with an overall flow control logic that controls the transfer of data to or from the various AGP devices and the standard AGP bus that is connected to the core logic of the computer system. The AGP to AGP Bridge can utilize a standard 32-bit AGP bus as well as (two) dual 32-bit buses to enhance bandwidth. In an alternate embodiment of the invention, the dual 32-bit buses can be combined to form a single 64-bit bus to increase the available bandwidth. Alternate embodiments of the AGP to AGP Bridge can accommodate the single 64-bit AGP bus for increased performance. Another alternate embodiment can accommodate peer-to-peer transfer of data between AGP busses on the bridge.